MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Computer Architecture**			**Module Delivery**	
Module Type	**Core**			☒ **Theory** ☒ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	**COMP31**				
ECTS Credits	**5**				
SWL (hr/sem)	**125**				
Module Level	3		**Semester of Delivery**	5	
Administering Department	Computer Science		**College**	College of Sciences	
Module Leader	Dr. Safaa H. Shwail		**e-mail**	safaa.husseinshwail@nahrainunive.edu.iq	
Module Leader's Acad. Title	Lecturer		**Module Leader's Qualification**	Ph.D.	
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name	Name		**e-mail**	E-mail	
Scientific Committee Approval Date	01/06/2023		**Version Number**	1.0	
Laboratory Techers	Dr. Safaa H. Shwail & Ass. Lec. Hanaa Mohamed & Ass. Lec. Zainab Haider				

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	1. Give a complete knowledge about how to represents data inside the computer system, floating point representation, and error detection method. 2. How the data transfer between the processor's registers and main memory and how to implement the arithmetic and logic micro-operations. 3. How to design and organization a basic computer, micro-programmed control, central processing unit, I/O organization, pipeline and vector processing, and multiprocessors.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Fixed-Point and Floating-Point Representation 2. Other Binary Codes and Error Detection Codes and its architecture 3. Register Transfer, Bus and Memory Transfers, and Arithmetic Microoperations 4. Binary Adder, Binary Adder-Subtractor, Binary Incrementor, and Arithmetic Circuit 5. Logic Microoperations, Some Applications, Shift Microoperations 6. Instruction Codes, Stored Program Organization, Indirect Address 7. Computer Registers, Common Bus System, Computer Instructions 8. Timing and Control, Instruction Cycle, Determine the Type of Instruction 9. Register-Reference Instructions, and Memory-Reference Instructions, Input-Output and Interrupt 10. Control Memory, Address Sequencing, Conditional Branching, Mapping of Instruction, Subroutines, Control Word 11. Stack Organization, Reverse Polish Notation 12. Input-Output Interface, I/O Bus and Interface Modules, I/O versus Memory Bus, Isolated versus Memory-Mapped I/O, Example of I/O Interface 13. Asynchronous Data Transfer, Asynchronous Serial Transfer, and Modes of Transfer 14. Parallel Processing and Pipelining
Indicative Contents المحتويات الإرشادية	Learning how the computer represent Floating-Point binary numbers. Exploring Other Binary Codes and Error Detection Codes and its architecture. Learning how to design Binary Adder, Binary Adder-Subtractor, Binary Incrementor, and Arithmetic Circuit. Exploring Timing and Control, Instruction Cycle, Determine the Type of Instruction. Knowing Register-Reference Instructions, and Memory-Reference Instructions, Input-Output and Interrupt. Learning the Control Memory, Address Sequencing, Conditional Branching, Mapping of Instruction, Subroutines, Control Word. Recognizing the Asynchronous Data Transfer, Asynchronous Serial Transfer, and

	Modes of Transfer.

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is by explaining lectures in an interactive way by letting the students to participate in the presenting through questions and answers while at the same time refining and expanding their critical thinking skills. This will be achieved through classes and labs.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	64	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	7
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	61	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	6
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	125		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	4	10% (10)	2,5,8,12	All
	Assignments	2	5% (5)	5,10	All
	Projects / Lab.	1	15% (15)	Continuous	All
	Report	1	10% (10)	10	All
Summative assessment	**Midterm Exam**	2 hr	10% (10)	7,14	All
	Final Exam	3hr	50% (50)	15	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Fixed-Point Representation Floating-Point Representation Other Binary Codes Error Detection Codes and its architecture
Week 2	Register Transfer Bus and Memory Transfers Arithmetic Microoperations Binary Adder Binary Adder-Subtractor
Week 3	Binary Incrementor Arithmetic Circuit Logic Microoperations Some Applications Shift Microoperations
Week 4	Instruction Codes Stored Program Organization Indirect Address Computer Registers Common Bus System Computer Instructions Instruction Set Completeness
Week 5	Timing and Control Instruction Cycle Determine the Type of Instruction Register-Reference Instructions Memory-Reference Instructions Input-Output and Interrupt Complete Computer Description
Week 6	Control Memory Address Sequencing
Week 7	Conditional Branching Mapping of Instruction Subroutines
Week 8	Mid-term Exam 1
Week 9	General Register Organization Control Word Examples of Microoperations
Week 10	Stack Organization Reverse Polish Notation
Week 11	Input-Output Interface I/O Bus and Interface Modules *I/O* versus Memory Bus Isolated versus Memory-Mapped I/O
Week 12	Example of I/O Interface Asynchronous Data Transfer

	Asynchronous Serial Transfer Modes of Transfer
Week 13	Parallel Processing
Week 14	Pipelining
Week 15	Mid-term Exam 2
Week 16	Preparatory week before the final Exam

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: what is assembly language? inside the cpu, general purpose registers
Week 2	Lab 2: segment registers, special purpose registers, Memory Access
Week 3	Lab 3: MOV instruction, Variables
Week 4	Lab 4: Arithmetic Instructions
Week 5	Lab 5: Logic Instructions
Week 6	Mid-Term Exam 1
Week 7	Lab 6: Labels, Control flow program
Week 8	Lab 7: Conditional and non conditional jump
Week 9	Lab 8: Loop instruction
Week 10	Lab 9: Factorial, Power, Summation
Week 11	Lab 10: Arrays
Week 12	Lab 11: Library of common functions - emu8086.inc
Week 13	Lab 12: Array exercises
Week 14	Lab 13: Review
Week 15	Mid-Term Exam 2

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	Computer System Architecture, 3rd edition, by M. Morris Mano	No

Recommended Texts		No
Recommended Texts		No

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.